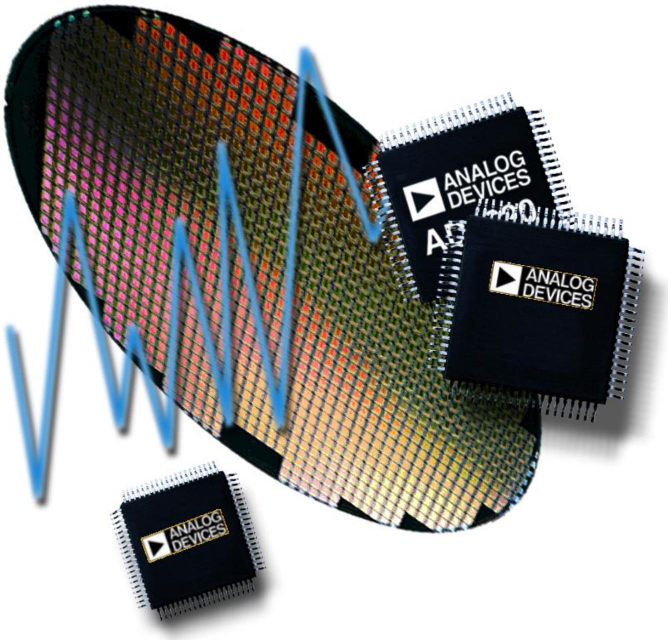

Reliability Report

Report Title: ADG5207 5x5 LFCSP at JC2 Qualification

Report Number: 20397

Revision: A

Date: 26 May 2023

Summary

This report documents the successful completion of the reliability qualification requirements for the release of 5x5 LFCSP package at JCET(JC2). The ADG5207 is a monolithic CMOS analog multiplexer comprising of 8 differential channels. The ADG5207 switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines, A0, A1, and A2.

An EN input on the device enables or disables the device. When EN is low, the device is disabled, and all channels switch off. The ultralow capacitance and charge injection of this switch makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make this device suitable for video signal switching.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.8 - 2.0um CMOS

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADG5207
Die Id	8YM21 A
Die Size (mm)	2.12 x 3.06
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	0.8 - 2.0um CMOS
Die Substrate	Si
Metallization / # Layers	AlSi(1.0%)Cu(0.5%)/2
Passivation	undoped-oxide/OxyNitride

Package/Assembly Product Characteristics

Table 2: Package/Assembly Product Characteristics - 32-LFCSP at JCET (JC2)

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADG5207
Package	32-LFCSP
Body Size (mm)	5.00 x 5.00 x 0.75
Assembly Location	JCET (JC2)
MSL/Peak Reflow Temperature(°C)	3 / 260°C
Mold Compound	Sumitomo G700LA
Die Attach/Underfill/TIM	Ablestik EN4300
Leadframe Material	Copper
Lead Finish	100Sn
Wire Bond Material/Diameter (mils)	4N Gold / 0.80

Package/Assembly Test Results

Table 3: Package/Assembly Test Results - LFCSP at JCET (JC2)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADG5207	Q20397.1.HS1	0/77
Solder Heat Resistance (SHR)	J-STD-020	MSL-3	ADG5207	Q20397.1.SH1	0/11
				Q20397.2.SH2	0/11
				Q20397.3.SH3	0/11
Temperature Cycling (TC)[1]	JESD22-A104	-65°C/+150°C, 500 Cycles	ADG5207	Q20397.1.TC1	0/77
				Q20397.2.TC2	0/77
				Q20397.3.TC3	0/77
Unbiased HAST (UHST)[1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADG5207	Q20397.2.UH1	0/77
				Q20397.2.UH2	0/77
				Q20397.3.UH3	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 4: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	ADG5207	32-LFCSP	JS-002	1Ω, Cpkg	±1250V	C3

Approvals

Reliability Engineer: Pernell Marc Mosuela